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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,343	02/05/2002	Mark Allen Silla	550-311	9811

7590 01/28/2005

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EXAMINER	
ELAMIN, ABDELMONIEM I	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 01/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,343	SILLA ET AL.	
	Examiner	Art Unit	
	A Elamin	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims *1-21,* are rejected under 35 U.S.C. 102(e) as being anticipated by Nowka, US. Pat. No. 6,545,512.

3. Claims *1, 11 and 21*, Nowka teaches a data processing apparatus [*title, abstract*], comprising:

a dynamic node [*dynamic node 250 of Fig. 2, col. 2, lines 3-4*];

precharge circuitry [*col. 2, lines 4-8*] arranged during a precharge phase to precharge the dynamic node to a first voltage level [*col. 1, lines 14-16*];

evaluation circuitry [*evaluation timing circuitry 220 of Fig. 2*] arranged to receive a number of input signals [*Fig. 2, col. 5, lines 12-15*] and during an evaluate phase to selectively drive the dynamic node to a second voltage level dependent on the input signals [*abstract, col. 5, lines 12-15*]; and

power down drive circuitry [*sleep circuitry 228 of Fig. 2*] arranged when the data processing apparatus is to enter a power down mode to drive the dynamic node to the second voltage level [*abstract, col. 2, lines 8-16, col. 5, lines 20-24*].

4. Claims *2 and 12*, Nowka teaches the power down drive circuitry comprises first circuitry responsive to a power down signal indicating that the power down mode is set to drive the dynamic node to the second voltage level and second circuitry [*sleep circuitry 228 of Fig. 2*] responsive to said power down signal to prevent the precharge circuitry from precharging the dynamic node to the first voltage level [*col. 2, lines 25-43*].

5. Claims *3 and 13*, Nowka teaches the first circuitry comprises an N type device connected between the dynamic node and the second voltage level [*210 of Fig. 2, col. 3, line 33*].

6. Claims *4 and 14*, Nowka teaches the second circuitry is arranged to receive the power down signal and a precharge signal indicating whether the precharge phase is active, and to generate as its output an input signal to the precharge circuitry, such that when the power down signal indicates that the power down mode is set, the output signal from the second circuitry is arranged to cause the precharge circuitry to be turned off [*col. 2, lines 25-43*].

7. Claims *5 and 15*, Nowka teaches the precharge circuitry comprises one or more P type devices, and said second circuitry is arranged to apply a logical OR gate function to the power down signal and the precharge signal [*Fig. 2, col. 2, lines 43-50, col. 3, lines 46-58, col. 3, lines 28-35*].

8. Claims *6 and 16*, Nowka teaches the second circuitry is positioned in series with the precharge circuitry between the dynamic node and the first voltage level, the second circuitry being arranged to turn off when the power down signal indicates that the power down mode is set, thereby preventing the precharge circuitry from precharging the dynamic node to the first voltage level [*Fig. 2, col. 2, lines 43-50, col. 3, lines 46-58, col. 3, lines 28-35*].

9. Claims *7 and 17*, Nowka teaches the first voltage level represents a logic 1 level [*high voltage state, col. 1, Lines 15-16*] and the second voltage level represents a logic 0 level [*low voltage state, col. 1, lines 17-20*].

10. Claims *8 and 18*, Nowka teaches the evaluation circuitry comprises a plurality of N type devices [*see evaluation timing circuitry 220 of Fig. 2*].

11. Claims *9 and 19*, Nowka teaches the precharge circuitry comprises one or more P type devices [*see precharge circuitry 221 of Fig. 2*].

12. Claims *10 and 20*, Nowka teaches a voltage regulating circuitry arranged when the data processing apparatus is to enter the power down mode to reduce the difference between the first voltage level and the second voltage level, thereby reducing leakage current through the precharge circuitry [*col. 1, lines 21-30, col. 2, lines 31-37 and col. 4, lines 27-34*].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A Elamin whose telephone number is (571) 272-3674. The examiner can normally be reached on MON-FRI 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A Elamin
Primary Examiner
Art Unit 2116

January 27, 2005